

FIG. 2: prior art

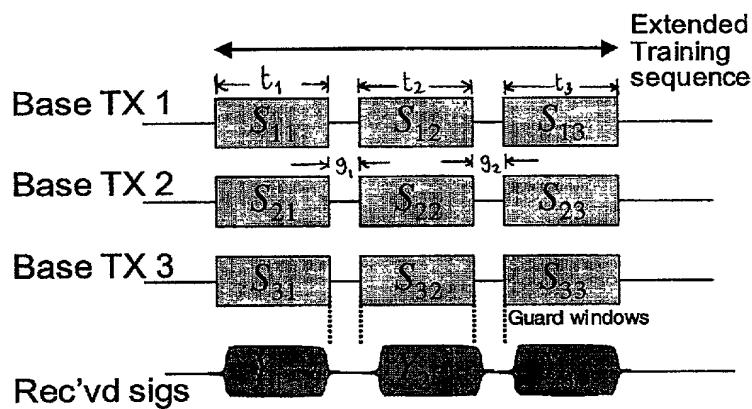


FIG. 4

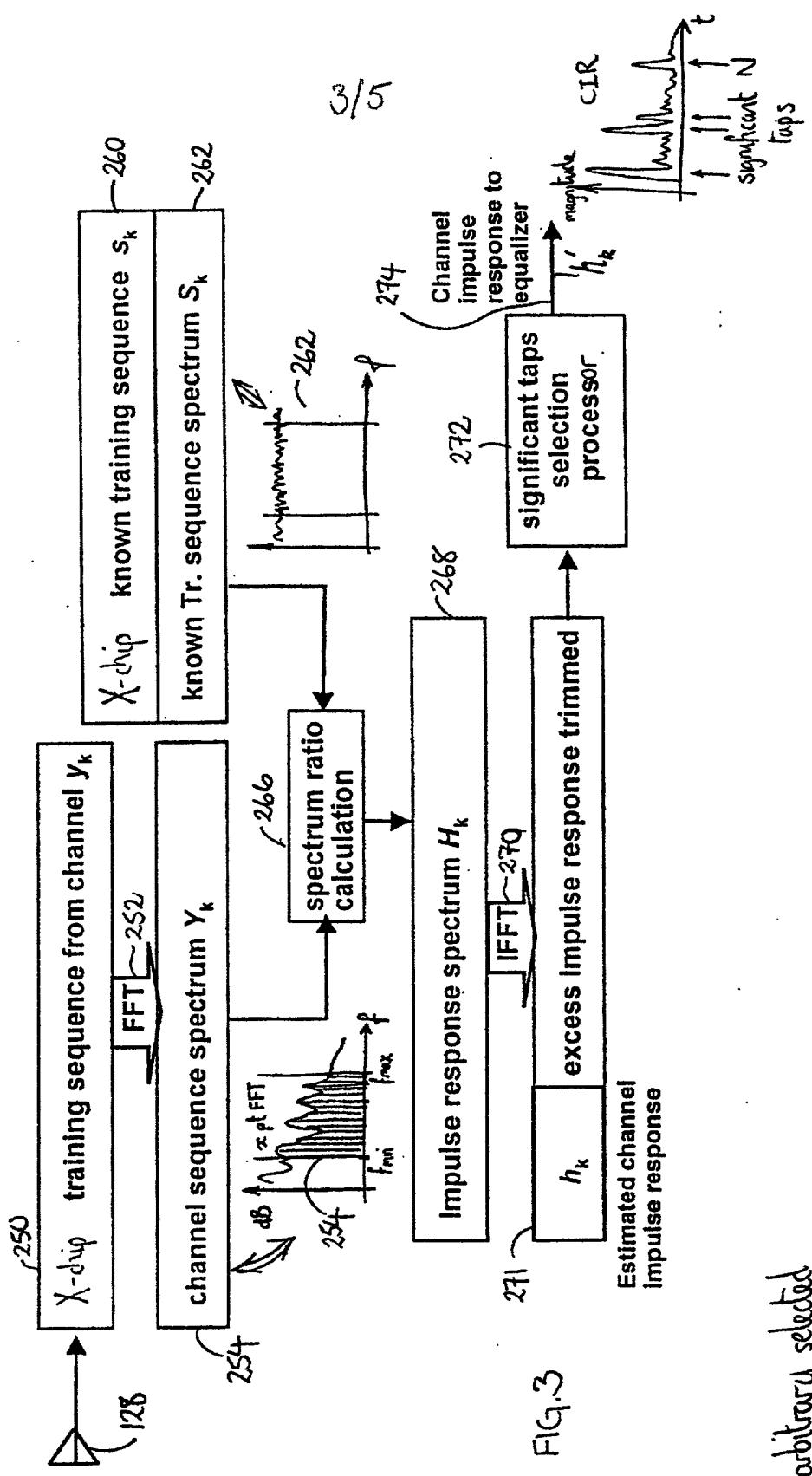


FIG.3

X =arbitrary selected
number of chips in training
sequence set by system standard.

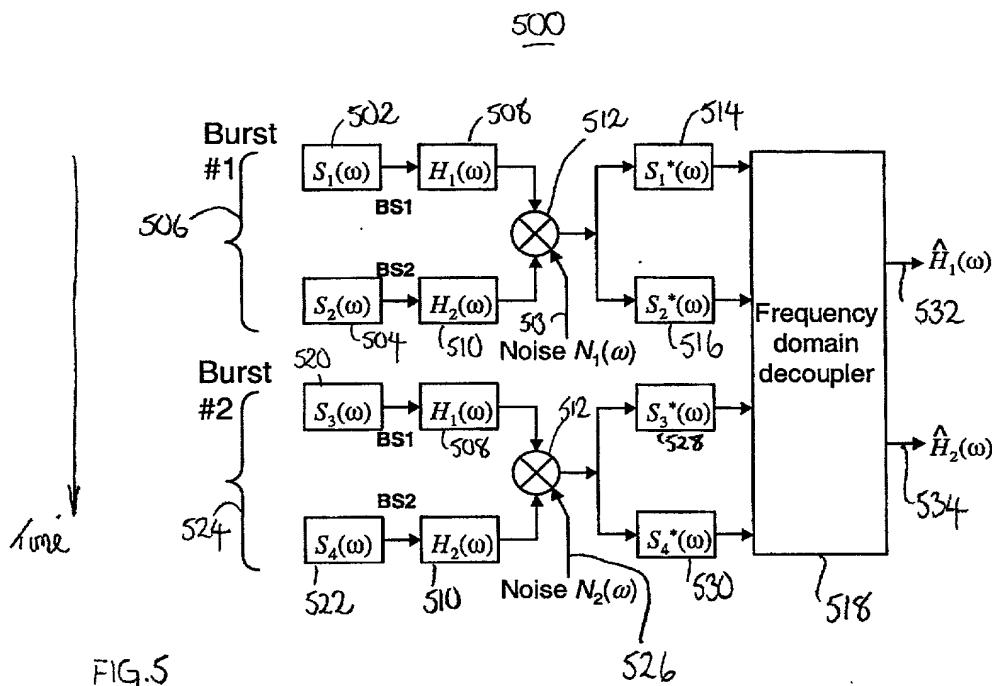


FIG.5

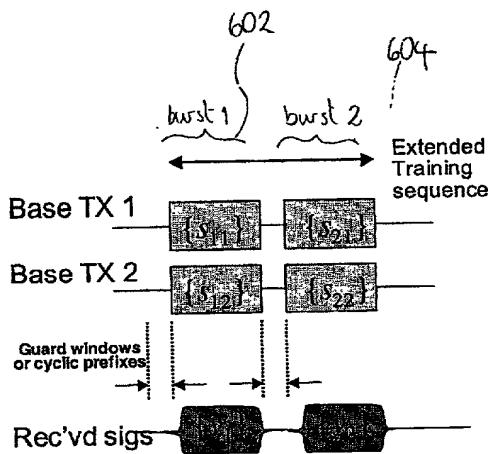


FIG.6

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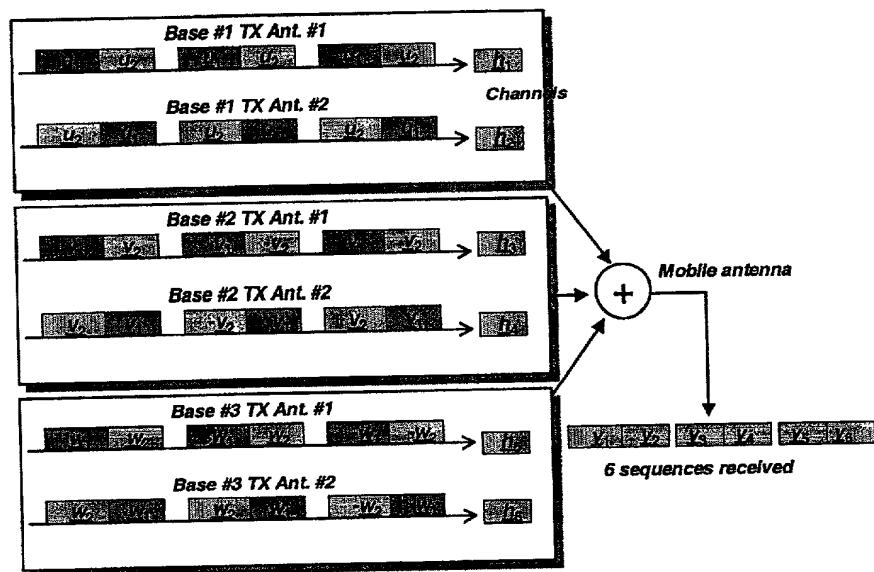


FIG.7